PRX 205

REFERENCE MANUAL

PART H_1

HARDWARE

SECOND EDITION

N.V. PHILIPS' TELECOMMUNICATIE INDUSTRIE-HILVERSUM - NEDERLAND
NETHERLANDS

37 315 31.0

INTRODUCTION

The reports H-1 and H-2 contain in a shortened version the functional characteristics of the PRX 205 system as far as they are of common interest.

Part H-1 gives general information on PRX and describes the control equipment from the Central Control unit up to and including the subsystems plus the utility functions.

Part H-2 describes the peripheral cabinets, the various switching networks and all types of Junctors, senders, receivers and test equipment. Both parts will be kept up to date by adding or modifying pages as soon as new data become available.
Changes will further be indicated by means of a vertical line in the right hand margin.
Please destroy the obsolete pages.
All remarks regarding additions, omissions or errors regarding part 1 should be directed to

ir. J.A. Brakel BE 604
tel.ext. 7327

and regarding part 2 to Mr.M. Koeman BE 510
tel.ext. 7501

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PRX 205

Hardware Manual

Modifications and additions

Extensive changes in the PRX hardware during the past year make it advisable to start a completely new edition of the Hardware Manual. This edition (report nr. 820) will gradually replace the first one (report nr. 200).

Mainly it will describe the version to be installed in the Overvecht exchange. Differences with the laboratory model will be indicated.

At the same time, the distribution will be changed. The number of copies has become so large, that updates take four to six weeks to be processed. This number will be reduced notably by issueing only one copy per office (to a maximum of 5 users). A few extra copies will be available in the secretary's office which can be borrowed on a weekly basis.

New pages:

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PRX 205

HARDWARE MANUAL PART I

MODIFICATIONS AND ADDITIONS

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Cancelled pages 217 - 221 - 231 and 242 will be inserted in the Testfloor Manual SR 2228-ML-H4414.

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SURVEY OF THE PRX 205 SYSTEM

1. Introduction

The PRX telephone switching system with stored program control is designed for public exchanges and the 205 version in particular for application in the local area. The adjective semi-selectronic indicates, that basically only "electronic" components are used namely integrated circuits and mini-reed contacts. In the development phase of the hard- and software philosophy of the system advantage was taken of the experience obtained with the full-electronic exchange system ETS III, of which two trial exchanges are in operation in Denmark and the Netherlands, and the message-switching system DS 714 with stored program control.

2. Design objectives

In addition to the usual requirements which a telephone system has to meet, the following aspects have been specifically considered in the design.

a) Network flexibility. The system can cope with divergent situations ranging from a simple subscriber terminal exchange to either a main transit center in a large local network of several exchanges or a combined local and trunk exchange. This is achieved by arranging the switching network as a transit center and the use of separate concentration stages for the subscriber lines. A modified subscriber concentration stage can be located as a dependent concentrator, which is remotely controlled by the PRX exchange acting as a parent exchange.

b) Signalling. The system has the ability to communicate using signalling systems of the conventional and modern type, such as M.F.C., P.C.M., tone push button-dialling and indialling in PABX's. Moreover special attention is given to cooperation with data-links of different kind such as common data channels (PCM or CCITT no. 6), links to and from administrative and/or maintenance centers, control links to dependent concentrators, remote controlled exchanges etc. For this reason the in- and output channels of the Central Control are structured to handle data words in a flexible and efficient way.

c) Central Control. As Central Control a general purpose computer has been chosen, and optimized to meet the real-time requirements set by the control of a telephony system. The stored program conception offers, besides the general system flexibility, a number of new features as:

(i) Simplification of the hardware contained in the circuitry of the switching network (relaysets, receivers, etc.), since, in principle no logic functions are required. This results in reduced costs and smaller space requirements.

(ii) Introduction of new subscriber facilities as automatic transfer, abbreviated dialling etc.

(iii) Extensive operational procedures on behalf of the

Administration such as, for instance, programs for traffic measurements and observation and routines by means of which programs may be introduced and data (e.g. classes of service, routing analysis) changed or other data (e.g. meter fee registrations, results of traffic measurement or observation) retrieved from the Central Control in a simple and easy manner.

(iv) Significant reduction of system maintenance due to a large package of fault detection, fault location and routine-test programs.

The majority of administrative and maintenance programs are infrequently used and are therefore not permanently housed in the Central Control, but can be transferred, together with input and result data, to and from a remote administrative or maintenance center via a data-link. This is not only of importance for the unattended operation of the system but also improves the economy of small exchanges by reducing the required storage capacity. It is obvious that these properties can only be achieved by the application of electrically modifiable memories.

d) Components. Not only in the central processors, but throughout the system, electronic circuitry is based to a great extent upon the use of integrated circuit blocks of one TTL-family with low dissipation. The "hard" contact functions in the switching network are performed by means of sensitive relays with mini-reedcontacts. This philosophy allows a reduction of dimensions, compared with conventional exchanges, by a factor of two to three, without the need for forced cooling inside the cabinet. Furthermore the overall power consumption of the system is reduced. By the exclusive use of sealed contacts the requirements for the environmental conditions in the equipment room, such as relative humidity and dust are greatly lessened.

e) System reliability. The required reliability for an uninterrupted service is attained by independent duplication of all equipment common to more than a limited number of peripheral circuits e.g. 64 subscribers. Routines in hard- and software ensure the rapid detection of a failure and the automatic change over of duplicated parts. As the most reliable solution for the Central Control the synchronous parallel operating mode, in which both processors are continuously compared, has been chosen. Moreover the system hardware itself has a high quality due to the derating of component parameters, a worst-case design and the application of reliable long-life components, sealed reed-contacts, wrapped wire connections, flow-soldered printed-wiring boards and connectors with rolled gold contacts.

f) Transmission quality. The system provides improved transmission properties by the smaller dimensions, careful design of the switching network and the use of transformer-coupled transmission bridges. The reed-contacts produce very little noise, particularly at low tone levels, which is advantageous not only for speech but especially for low level signals as used in M.F.C., tone push-button dialling and data transmission.

g) Mechanical design. The construction of cabinets and units is made relatively simple by modular design, emphasized standardisation rules and the assembly of all components on plug-in printed-wiring boards. In connection with a wrapped-wiring technique, which can be mechanised, and automatic test procedures, this leads to an efficient and uniform manufacture. As a further

consequence these aspects, together with prewired cabinets, intermediate distribution frames incorporated in the equipment cabinets and, in the control part of the system, the use of connector terminated cables,, allow an important reduction in the time required for the on site installation, expansion and testing of the system.

h) Economy. The system is competitive with conventional exchanges but the presence of the Central Control will restrict the economic capacity downwards to a minimum of between 1000 and 2000 subscribers. This advantageous underlimit is gained by optimizing the traffic handling capability of the Central Control for medium rather than large sized exchanges, from which emerges the choice of the relative small wordlength of 16 bits, the basic instruction cycle time of 2 microseconds and the expansion of the storage capacity by modules of 16.000 words. For large exchanges the system provides two solutions namely the introduction of more processor-pairs, which share the system load, or a more powerful machine with e.g. a reduced cycle-time and wider wordlength, but whose software and channel structure will be compatible with the slower version.

3. System description

3.0. Configuration. The system, as shown on page 110 comprise four main parts viz. the Switching Network (including datalinks), the "Utility" equipment, the Interface Equipment and the Central Control. For the transfer of information to and from the interface two highways with different speeds are available, namely a system control channel and system data channel.

3.1. Switching Network. The heart of the network is a four-stage link switching network composed of identical expanding and compressing "transit blocks" which contain two stages for 64 lines. The intermediate distribution frame between the blocks allows, without the use of multiples, a gradual expansion of the system to a maximum of about 800 lines (with the indicated expansion factor 8 by 12). For larger exchanges an additional "mixing" block with two stages, as shown in dotted lines, is incorporated which increases the maximum of the total transit block (now six stages) to 4000 lines. The illustrated configuration is practicable if the majority of the trunk lines are used "one-way", but in the contrary situation a "both-way" solution is possible by also interlinking the left-hand and right-hand blocks. The relaysets required for trunk lines from other exchanges and remote concentrators, for lines direct from large PABX's and for junctions from the subscriber local blocks are intermixed and connected to the transit blocks via an I.D.F. The same applies for the outgoing sets. This improves the traffic overload properties and makes the system independent of the division between originating, terminating and transit traffic.

The receivers and senders for M.F.C., tone push button-dialling (2 times 1 out of 4) and PABX in-dialling (slow D.C. loop pulsing or fast tone p.b. dialling) are connected to the transit blocks in the same manner as the relaysets and are temporary switched through to them during the processing of a call. This solution is not only flexible, but avoids the application of inefficiently used separate concentration networks. The "local block" contains a three stage network and concentrates a group of max. 512 subscriber and PABX-lines to 64 outlets; the outlets of one or two blocks are combined in accordance with standard multiple arrangements and lead to two

groups of junctors AJ and BJ, for originating and terminating traffic respectively. In the first (subscriber) stage transposition is applied while the network shown allows an average total traffic per line of 0,07 Erl. By simply adding (prewired cabinet) 8 by 4 switches in parallel to the existing ones in the third stage this maximum is increased to 0,13 Erl. For larger traffic a second type of block is available, which differs only in the first stage and has corresponding maxima of 0,14 and 0,28 Erl. respectively.

Throughout the speech path network two types of plug-in units, comprising one 8 by 8 or two 8 by 4 matrices, are used; by connecting them in parallel all required switch sizes can be made as 8 by 12, 8 by 16 etc.

In the first subscriber stage a third type of matrix unit is necessary as this incorporates the line circuit components (fig. 2 on page 107) A unit contains 64 relays with three reed-contacts and 64 diodes for access to the marker. Inside a multi-stage block the third contact is used during the marking process and to convey the holding current for the relays, which are kept in series.

Outside the blocks however all the interconnections in the switching network are on a two-wire basis, which allows a fully independent control and operation of all the devices and consequently a great flexibility in the call processing. The free/busy states of all the devices and links and the current interrelationships between them are contained in the memory of the Central Control in the form of a "System Map".

The individual character and reliability of the devices and speech paths allow a check procedure on a periodical basis by means of automatic routine tests.

The data links used for the transfer of information to and from other exchanges and maintenance and/or administrative centers are ordinarily of the half-duplex type with transfer rates ranging from 50 to 2000 Baud. Functions such as packing and unpacking of data words, storage of messages etc. are performed by the Central Control, resulting in simplified data terminals.

3.2. Utility. In addition to the data links and the control and display panels of the Central Control, there is the "Utility" equipment, which provides the local man - machine communication means in the system for operational and maintenance purposes. In an unattended exchange this equipment is restricted to a teleprinter with low-speed reader and punch. Sometimes a high-speed papertape reader is present during a short period after the introduction of a program change in order to reload the operational program. The magnetic tape-units, lineprinter etc. are mainly used in a off-line configuration of the Central Control for the assembly of programs, program debugging, etc.

3.3. Interface. This equipment consists of the control devices for the switching network, data links and utility equipment and also of bus terminals which convert the information transferred between the central processor and the controls. A number of controls are in common to a terminal and each of them is duplicated according to the stand-by principle. During the call-processing they are continuously checked in combination with automatic switch-over procedures (functional and parity checks). The controls for the data links and utility are mainly "active" and have the ability to transfer autonomously information to and from the central processors while

those for the switching network are "passive" and under direct control of the processor. The last group consists of three types.

a) Tester (fig. 3). The matrix is arranged in groups of 16 points in parallel, mostly of the same category, which can be freely addressed by interrogation instructions from the processor. The test result is transferred to the processor and used as "last look" condition during call processing or, if it is part of a scan procedure, compared with the previous result stored in the memory.
The scan rate and sequence are determined by the processor. The singlefold matrix is checkd by testing "dummy" groups with preset conditions and is independently subdivided to restrict a fault to a small group of peripheral circuits.

b) Driver (fig. 4). The so-called "slow" driver contains duplicated buffer registers and address decoders controlling singlefold reed relay matrices for access to the relaysets in the switching network. These matrices are subdivided for the reasons already mentioned. Depending upon the switching instructions received a relay can be operated or released in a few msec. In the case that very stringent real time requirements occur a "fast" driver is used in which the relay matrix is replaced by flip-flops, individual per command and per device, followed by relay-drive stages. The operating time for set and reset orders is in the same magnitude as for the tester viz. a few microseconds.

c) Marker (fig. 2). Since the free-path selection is performed by the Central Control, the marker is basically a "slow" driver with the difference that a number of relays are operated in series. The matrices give access to the outlets and the multipled "vertical" control wires of the network via which the crosspoint relays are operated stage for stage in a coincidence arrangement. The whole control network is sub-divided for reliability reasons, while checks prevent that new connections are unwantedly switched to a standing connection as a result of a fault. The marker has also the task of releasing a standing connection. Its overall operating time is smaller than 12,5 msec. for TB operation and 37,5 msec. for LB operation.

3.4. System Channels. For the connection of the Central Control to the interface equipment the so-called Control and Data Channels are available. The duplication of these channels and the accessibility of each processor to each channel terminal assures the reliability of this part of the system.

a) Control Channel. This channel is designed for general use in the system and bridges long distances at a basic speed of 60.000 words per sec. in spite of the relatively high-noise environment of a telephone exchange. Therefore the buslines (twisted pair) are coupled by transformers in the terminals with as an additional advantage the insensitivity for ground potential differences. Each bussystem comprises 16 data and 8 address lines outgoing (from Central Control) and 16 data lines incoming, accompanied by parity and control lines.

b) Data Channel. This channel is additionally introduced in relative large exchanges only if a great number of datalinks for "common channel signalling" occur or is used to connect the highspeed utility in a off-line configuration for program testing etc.
The basic speed of 500.000 words per sec. and the autonomous direct access to the memories reduce the loading of the central processor for data transports. The D.C. bussystem (coaxial) is restricted in

distance and consists of 16 data lines outgoing and 16 data and 17 memory address lines incoming, again accompanied by parity and control lines.

3.5. Central Control. The Central Control comprises the two realtime processors and the terminals for the system channels. The processors operate instruction synchronously and are continuously compared. The interconnections are designed such that each device is completely independent from the other ones. The "on-line" configuration is governed automatically by an alarm and switch-over device, and manually by the system panel. The main aspects will be briefly described.

a) Processor Terminal. This device provides as well as the terminals for the Control Channel the circuitry for interrups, (from interface equipment, central processors etc.) and requests (for autonomous data-word transports) on the Control Channel. Allotters (hardware) determine the priority between simultaneous interrupts or requests. Groups of interrupts are masked by a register which is set by program, according to its software priority.

b) Data channel Control. This equipment contains the circuitry for the terminals of the Data Channel and for its autonomous transport requests. Requests are allotted and data and addresses are checked before admitting them to the memory registers of the processors.

c) Input/Output Unit. The I/O unit is to some extent independent of its corresponding Central Processing Unit and allows an asynchronous cooperation with the Interface equipment. It contains six registers, three of which are used to store by program the information required for the autonomous scan procedure. This procedure reduces the loading of the CPU due to the fact that the I/O unit automatically increases the current address and seizes the CPU registers to perform compare, load and store functions at the moment that the new status of the interrogated peripheral points is received. Moreover a test-access connection to the other processor is provided via which a faulty processor can be investigated by means of diagnostic programs in the on-line machine.

d) Central Processing Unit. A binary one-address machine with a word and instruction length of 16 bits and 6 program-accessible registers. The instruction package comprises 25 memory reference and 43 logic, transfer and control instructions. Modification and indirect addressing is specified per instruction and in order to obtain full addressability relocation of the 8 bit address field is applied by adding the contents of a 17 bits relocation register, which is loaded per program module. Interrupts and autonomous transports and scans, received via the I/O unit have hardware priority over instructions. After each completed instruction the control decides what the next operation shall be (program "hesitating"). A control panel is provided for manual operations.

e) Memory. The capacity is extensible to a maximum of 8 modules of 32.000 words each. A module contains a stack of ferrite-core matrices (30 milcore) driven according to the coincident-current principle with a common current source, which allows a dissipation as low as 60 Watts. Access time to any word is 600 nanoseconds and the read-write cycle takes 2 microseconds. The cooperation with the CPU is asynchronous by means of the processor stop clock facility. The Data Channel has access priority over the CPU and operates with the cycle-stealing principle. The memory is used "unstratified" for program and data.

but a write protect bit per word is used to avoid mutilation of programs or fixed data. Moreover, protected areas are reserved for data channel transports and special programs, such as "bootstrap" etc. For reliability reasons a parity check on read-out and a power failure protection are provided.

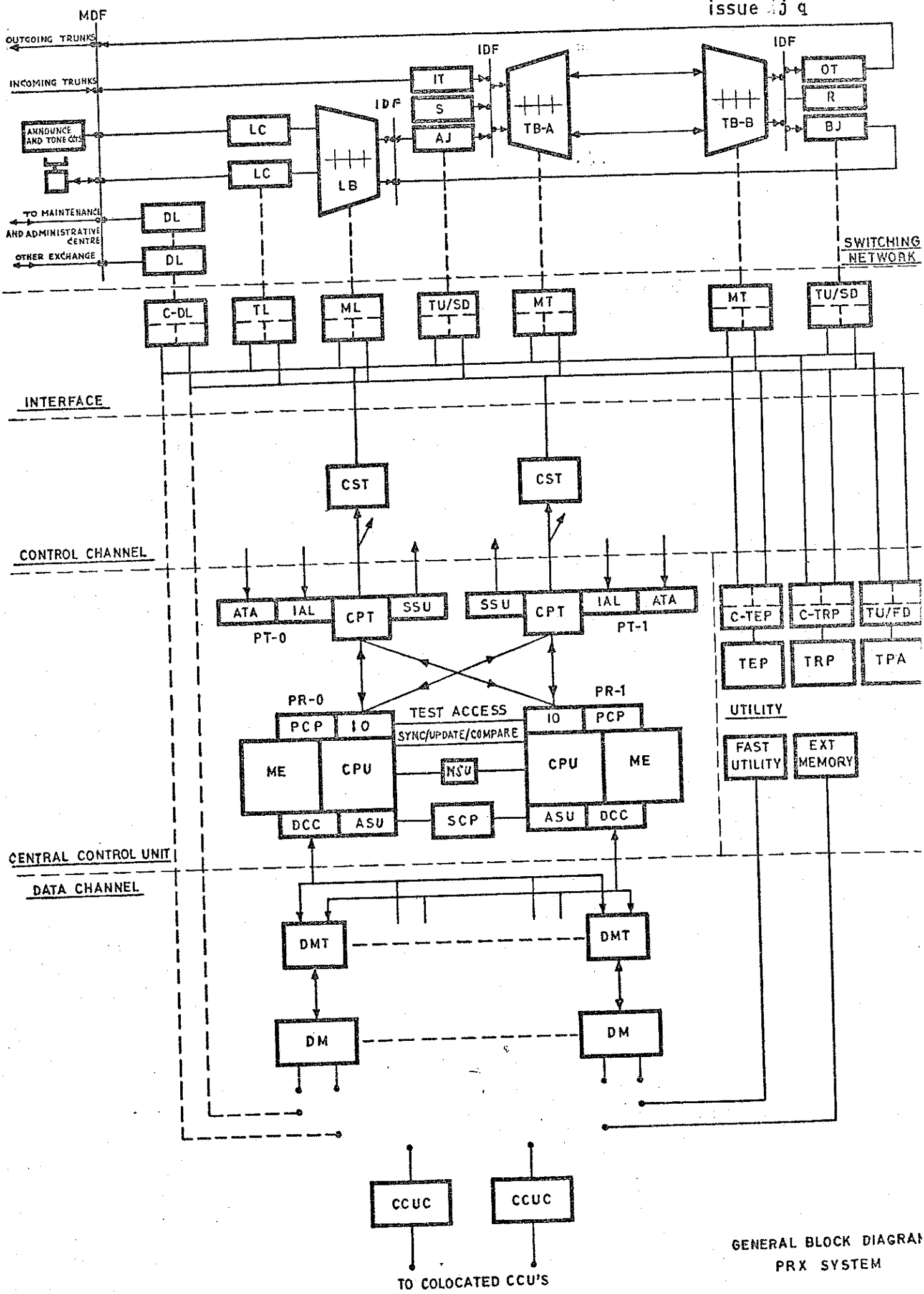
f) Dual operation and alarm c.q. switch-over functions. Both processors act synchronously and are compared one or more times per instruction via the compare channel between the C.P.U.'s. If a disagreement occurs a test program is initiated in both processors which then independently search for the error; the failing one is automatically taken out of service. After repair the memory of the off-line machine is completely updated by means of a low-priority program in the on-line processor via the update (previously compare) channel. Finally this processor is automatically switched to the online dual situation. If, after the introduction of a program change, both processors should fail on program errors, an automatic restart and recovery is initiated by an external fail-safe device.
Only one of the terminals of a system channel is active to both processors and this configuration is switched periodically by program for checking purposes. The configuration is automatically switched by the Alarm and Switch-over Unit, which is triggered by the various alarms in the Central Control such as compare-, parity-, clock-, and power failures. Manual control of the ASU is provided from the system panel.

g) Software. The programs, operational in the system, can be roughly arranged in three main groups for the call-processing, system assurance and man - machine communication respectively. The call-processing demands about 15.000 to 20.000 words, depending on the telephony requirements, and is written in relatively small modules for flexibility reasons. The programs are interlinked and scheduled, in accordance with their priority, by a master control program, which performs its task on the basis of the system and real time clock interrupts.
The set of programs, used to assure the reliable operation of the system, consists of programs for fault detection, monitoring, automatic switch-over procedures etc. By means of the man - machine communication programs data and programs may be introduced and changed for exploitational and maintenance purposes.

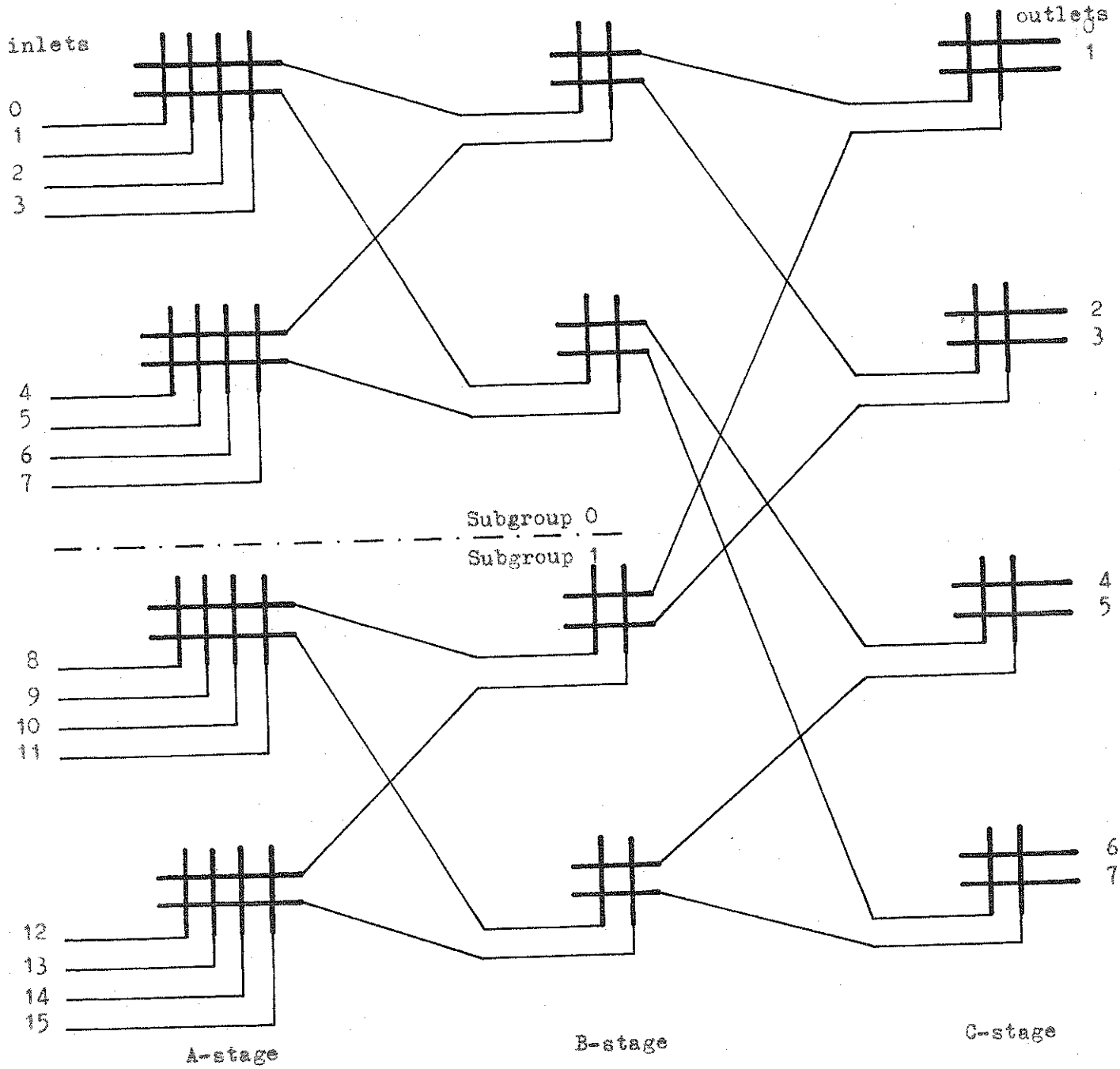
A large number of off-line programs, using together more words than are required for the call-processing, are provided on paper tape. These programs, such as routine tests, fault location procedures, traffic measurements etc. are loaded on demand in a reserved space of the memory.

4. Mechanical Design.

All equipment dimensions are based upon a modulus of 0,1 inch. The standard printed circuit board is 11 ins high and 9 ins deep and comprises for instance 64 crosspoint relays or 40 D.I.L. integrated circuit blocks. Eight shelves, each with 32 boards, are housed in a standard cabinet, 102 ins high, 57,4 ins wide and 15 ins deep.



GENERAL BLOCK DIAGRAM
PRX SYSTEM



Each + is a possible through-connection point.

Symbol: 4 | 2 2 | 2 2 | 2 General: Ai | Ao Bi | Bo Ci | Co

Concentration factor = $\frac{\text{inlets}}{\text{outlets}} = \frac{Ai \times Bi \times Ci}{Ao \times Bo \times Co} = 2$

Nr. of B - switches: Ao x Ci = 4

THREE - STAGE LINK NETWORK

STANDARD ABBREVIATIONS IN THE PRX 205 SYSTEM

The names are only functional names, for example to use as labels for the program modules, but not to indicate type numbers. In this way it is possible that one name is provided for two or more type numbers or one type number for two or more names.
For the **structure** of functional names and numbers: see **Procedures Manual**
For a complete up to date list of standard abbreviations: see ST515-1011.

Hardware

AJ	A junctor circuit
AJI	AJ in direct connection with an incoming PBX line
ASU	Alarm and switching unit
ATA	Autonomous transport allotter
BJ	B junctor circuit
BJØ	BJ in direct connection with an outgoing PBX line
CAB	**Cabinet**
CAD	Cathode ray display
CAP	Card punch
CAR	Card reader
CCH0	Control channel 0
CCH1	Control channel 1
CCU	Central control unit
CCUC	Central control unit coupler
CDL	Data link control
CLIP	Line printer control
CMTU	Magnetic tape unit control
CPT	Control channel processor terminal
CPU	Central processing unit
CSI	Control channel simulator
CST0	Control channel 0 subsystem terminal
CST1	Control channel 1 subsystem terminal
CTEP	Teleprinter control
CTRP	Paper tape reader and punch control

DGR0	Data channel group 0 (even channels)
DGR1	Data channel group 1 (odd channels)
DCC	Data channel control
DCH	Data channel
DL	Data link
DM	Data multiplexer
DMT	Data multiplexer terminal
DSI	Data channel simulator
DRU	Drum Unit
DRS	Drum Subsystem
DIU	Disc. Unit
DIS	Disc. Subsystem
FD	Fast driver
FDC	Fast driver control
FDM	Fast driver matrix
FR	Forward-release unit for ØT-F
FU	Fuse
MFU	Minor fuse
CFU	Cabinet fuse
SFU	Suite fuse
IAL	Interrupt allotter
IDF	Intermediate distribution frame
IFX	IDF connector, junctor side
IFD	IDF connector, SWD-side
IFE	IDF connector, SWE-side
IFF	IDF connector, SWF-side
IFG	IDF connector, SWG-side
IØU	Input/output unit
ISWA	Inlet of SWA
ISWD	Inlet of SWD
ISWF	Inlet of SWF
IT	Incoming trunk junctor circuit
ITF	IT for F line signalling
ITFH2	IT-F, hook signalling, 2 wire
ITFH3	IT-F, hook signalling, 3 wire
ITFM2	IT-F, metering, 2 wire
ITFM3	IT-F, metering, 3 wire
ITFB	IT-F with break-in and measuring facilities

ITL	IT for loop signalling and MFC
ITLH	IT-L, hook signalling
ITLM	IT-L, metering
LB	Line link block
LC	Subscribers line circuit
LPU	Line printer Unit
LPS	Line Printer Subsystem
KB	Keyboard
MAS	Mass (core) storage
MDF	Main distribution frame
MEM	Memory module (32K)
ML	LB Marker
MLC	LB marker control
MLM	LB marker access matrix
MR	Marker
MSU	Master switching unit
MT	TB marker
MTC	TB marker control
MTM	TB marker access matrix
MTU	Magnetic tape unit
MVx	Marker vertical access matrix to stage x
MTS	Magnetic Tape Subsystem
OSWC	Outlet of SWC
OSWE	Outlet of SWE
OSWG	Outlet of SWG
ØT	Outgoing trunk junctor circuit
OTF	ØT for F signalling
OTFH2	ØT-F, hook signalling, 2 wire
OTFHF	ØTF, hook signalling, 2 wire with forward release unit
OTFH3	ØT-F, hooksignalling, 3 wire
OTFM2	ØT-F, metering, 2 wire
OTFM3	ØT-F, metering, 3 wire
OTFMF	ØT-F, metering, 2 wire with forward release unit.

OTFP2	ØT-F, hooksignalling with P2 code, 2 wire
OTFP3	ØT-F, hook signalling with P2 code, 3 wire
OTFPF	ØTF, hook signalling with P2 code, 2 wire with forward release unit
OTL	ØT for loop signalling and MFC
OTLH	ØT-L, hook signalling
OTLM	ØT-L, metering
OUMF	Oscillator unit for MFC
OUKT	Oscillator unit for KT
PI	Printer Unit
PCP	Processor control panel
PGU	Power guarding unit
PME	Processor memory
PR	Processor
PRO	One processor of a pair
PR1	Other processor of a pair
PTO	Processor terminal 0
PT1	Processor terminal 1
PTP	Paper Tape Punch — used in DC17
PTR	Paper Tape Reader — used in DCH
R	Receiver
RKT	Receiver for keytone signalling
RMF	Receiver/Sender for MFC signalling (B-side of line)
RTS	Ringing and tone supply
SID	Signal Distributor
S	Sender
SCP	System control panel
SD	Slow driver
SDC	Slow driver control
SDM	Slow driver matrix
SKT	Sender for keytone signalling
SMF	Sender/Receiver for MFC signalling (A-side of line)
SN	Switching network
SP	Sender for P2 code signalling
SSL	Sender for subscriber loop signalling (ALS 70)
SSU	Subsystem switching unit
STC	System test coupler

SWA	Subscriber switch for LB
SWB	Intermediate switch for LB
SWC	Junctor switch for LB
SWD	Expansion switch for TB
SWE	Mixing switch for TB
SWF	Switch for MB, A-side
SWG	Switch for MB, B-side
TDP	Technical Display Panel
TAC	Test access circuit
TAP	Paper tape punch used in CCH
TAR	Paper tape reader used in CCH
TOD	Time of Day unit
TB	Trunk link block
TBA	TB at the A-side
TBB	TB at the B-side
TC	Tone circuit
TCNU	Number unobtainable tone circuit
TDC	Time-of-day clock
TEP	Teleprinter
TR	Tester
TRC	Tester control
TL	LC tester
TRM	Tester matrix
TU	Unit tester

12PS	Power supply unit +12V
5PS	Power supply unit + 5V
N5PS	Power supply unit - 5V
etc.	

REPORTS AND DESCRIPTIONS.

DATE	NUMBER	AUTHOR	TITLE
23- 2-71	SR 2228-884	de Vos	Legal and illegal instruction codes.
17- 3-71	SR 2228-595	Schuitemaker	The input-output unit of the PRX 205 processor (10-unit).
13- 3-71	SR 2228-362	Borcherding	Lijnstroomloop t.b.v. P.R.X.centrales
18-10-70	SR 2228-789	Scholte	M.F.C. Oscillatoren
29- 4-71	SR 2228-H961	Grevenstuk	The main differences between ø-model and the PRX-205 Utrecht (afterwards referred as Utrecht)
18-10-70	SR 2228-789	Hillekens	Ontvanger voor toondruktoetskiezen in P.R.X. 205 Tijdvak 1968 - 1970.
21-10-69	SR 2228-523	Borcherding	Het rangeren van transietverbindingen in het PRX-systeem
11- 9-70	SR 2228-756	du Mosch	Specificatie voor centrale signaalvoorziening t.b.v. P.R.X.
6-12-67	SR 2228-100	Keers	Some remarks on the Switching Network
29-10-69	SR 2228-530	Dekker	Integratie schakeling
24- 6-68	SR 2228-229	Statius Muller	Foutdetectie in het informatietransport systeem.
18-11-68	SR 2228-287	Borcherding	Het opbouwen en verbreken in het PRX-205 systeem.
22-11-68	SR 2228-291	Bohlmeijer	Stack 16K18 voor het PRX geheugen van PTI
14-11-68	2214-00-324	Bakvis	P.R.X. Verslag
22-11-71	SR 2228-1139	de Vos	PRX Design Considerations and Cycle Time study
12-10-71	SR2228-H1093	Brakel	Proposal for a numbering System and Extension sequence within the Central Control unit.
14- 6-71	SR 2228-1433	de Vos	Overvecht Field Measurement of Processor Cycle Time.
14- 6-72	ST 515-1011	v.d. Wilk	Abbreviations PRX systems.

ASCII/ISO / International Telegraph Alphabet no. 2

bit 7	0	0	1	1	
bit 6	0	1	0	1	
bits 1÷5	ASCII	ASCII	ASCII	ASCII	INT.TGF 2
0	NULL .	SPACE	@	` .	(code 32) .
1	SOH	! .	A .	a	E 3
2	STX	" .	B .	b	LF
3	ETX .	#	C	c .	A - .
4	EOT	$.	D .	d	SPACE
5	ENQ .	%	E	e .	S ' .
6	ACK .	&	F	f .	I 8 .
7	BELL	' .	G .	g	U 7
8	BS	(.	H .	h	CR
9	HT .	)	I	i .	D WRU .
10	LF .	*	J	j .	R 4 .
11	VT	+ .	K .	k	J BELL
12	FF .	,	L	l .	N , .
13	CR	- .	M .	m	F
14	SO	. .	N .	n	C :
15	SI .	/	O	o .	K (.
16	DLE	0 .	P .	p	T 5
17	DC_1 .	1	Q	q .	Z + .
18	DC_2 .	2	R	r .	L) .
19	DC_3	3 .	S .	s	W 2
20	DC_4 .	4	T	t .	H .
21	NAK	5 .	U .	u	Y 6
22	SYN	6 .	V .	v	P 0
23	ETB .	7	W	w .	Q 1 .
24	CAN .	8	X	x .	O 9 .
25	EM	9 .	Y .	y	B ?
26	SUB	: .	Z .	z	G
27	ESC .	;	[	{ .	FGRS .
28	FS	< .	\ .	¦	M
29	GS .	=	]	} .	X / .
30	RS .	>	^	~ .	V = .
31	US	? .	_ .	DEL	LTRS

. = Parity bit = for even parity; start = space = 0 = pos. voltage.
In ISO, char. within double line may be changed by national agreement.

ASCII/ISO - Abbreviations

NULL	Null, idle
SOH	Start of Heading
STX	Start of Text
ETX	End of Text
EOT	End of Transmission
ENQ	Enquiry
ACK	Acknowledge
BELL	Bell, audible signal
BS	Back space
HT	Horizontal Tab
LF	Line Feed
VT	Vertical Tab
FF	Form Feed
CR	Carriage Return
SO	Shift Out
SI	Shift In
DLE	Data Link Escape
DC1..4	Device Control
NAK	Negative Ack
SYN	Synchronous
ETB	End of Transmission Block
CAN	Cancel
EM	End of Media
SUB	Substitue
ESC	Escape
FS	File Separator
GS	Group Separator
RS	Record Separator
US	Unit Separator
DEL	Delete, idle

ITA #2 - abbreviations

LF	Line End
CR	Carriage Return
WRU	"Who are you?"
BELL	Audible signal
FGRS	Figure shift
LTRS	Letter shift

Teletype ASR codes

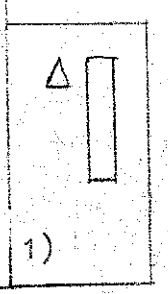
	printable characters			
bit 7	0	0	1	1
bit 6	0	1	0	1
bits 1 ÷ 5	ASCII	ASCII	ASCII	ASCII
0	NULL .	SPACE	@	
1	SOH	! .	A .	
2	STX	" .	B .	
3	ETX .	#	C	
4	EOT	$.	D .	
5	ENQ .	%	E	
6	ACK .	&	F	
7	BELL	' .	G .	
8	BS	(.	H .	
9	HT .	)	I	
10	LF .	*	J	
11	VT	+ .	K .	
12	FF .	,	L	
13	CR	- .	M .	
14	SO	. .	N .	
15	SI .	/	O	
16	DLE	0 .	P .	
17	DC_1 .	1	Q	
18	DC_2 .	2	R	
19	DC_3	3 .	S .	
20	DC_4 .	4	T	
21	NAK	5 .	U .	
22	SYN	6 .	V .	
23	ETB .	7	W	
24	CAN .	8	X	
25	EM	9 .	Y .	
26	SUB	: .	Z .	
27	ESC .	;	[	
28	FS	< .	\ .	
29	GS .	=	]	
30	RS .	>	^	
31	US	? .	_ .	DEL

. = Parity bit = 0 for even parity; start = space = 0 = pos. voltage.
11 in bit position 7 and 6 will be read as 10 by the printer, except for DEL

Olivetti Te 318 codes Model P1 of Olivetti Nederland BV

printable characters

bit 7	0	0	1	1
bit 6	0	1	0	1
bits 1÷5	ASCII	ASCII	ASCII	ASCII
0	NULL .	SPACE	@	.
1	SOH	! .	A .	
2	STX	" .	B .	
3	ETX .	#	C	.
4	EOT	$.	D .	
5	ENQ .	%	E	.
6	ACK .	&	F	.
7	BELL	' .	G .	
8	BS	(.	H .	
9	HT .	)	I	.
10	LF .	*	J	.
11	VT	+ .	K .	
12	FF .	,	L	.
13	CR	- .	M .	
14	SO	. .	N .	
15	SI .	/	O	.
16	DLE	Ø .	P .	
17	XON .	1	Q	.
18	TAPE .	2	R	.
19	XOFF	3 .	S .	
20	TAPE .	4	T	.
21	NAK	5 .	U .	
22	SYN	6 .	V .	
23	ETB .	7	W	.
24	CAN .	8	X	.
25	EM	9 .	Y .	
26	SUB	: .	Z .	
27	ESC .	;	[	.
28	FS	< .	\ .	
29	GS .	=	]	.
30	RS .	>	↑	.
31	US	? .	← .	DEL

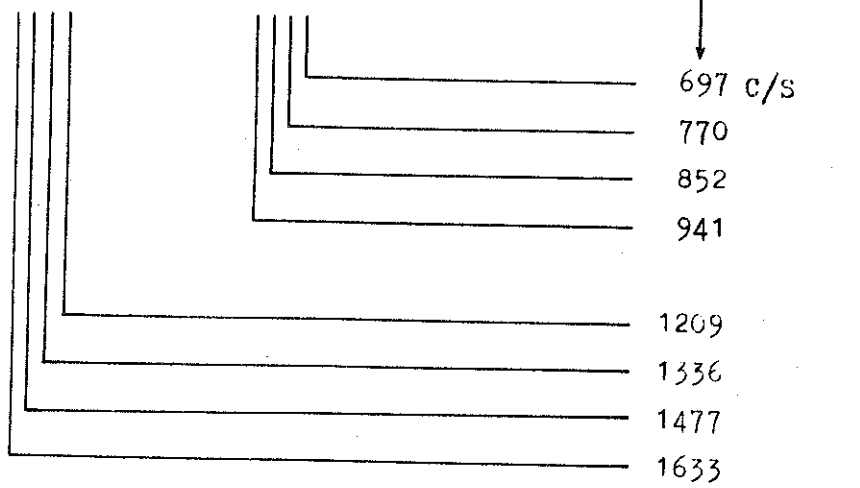
1) 

. = Parity bit = 0 for even parity; start = space = 0 = pos. voltage.

1) New Line Key generates the sequence CR-LF-DEL

Keytone signalling code

Value	High code	Low code	Bilinear
1	0001	0001	11
2	0010	0001	21
3	0100	0001	31
4	0001	0010	12
5	0010	0010	22
6	0100	0010	32
7	0001	0100	13
8	0010	0100	23
9	0100	0100	33
0	0010	1000	24
11	0001	1000	14
12	0100	1000	34
13	1000	0001	41
14	1000	0010	42
15	1000	0100	43
16*	1000	1000	44



* = 0 met blokkeerfunctie

MFC - codes

Forward signals:

Numerical signals: I - 1 ÷ I - 15
Character signals: II - 1 ÷ II - 15

Backward signals:

Proceed to send signals: A - 1 ÷ A - 15
Character signals : B - 1 ÷ B - 15

Equally numbered signals in all groups are composed in the same manner according to the following schedule:

	Forward freq.	1980	1860	1740	1620	1500	1380
	Backward freq.	540	660	780	900	1020	1140
	1st component	-	4	3	2	1	0
	2nd component	11	7	4	2	1	-
Code	Components						
1	0 + 1					x	x
2	0 + 2				x		x
3	1 + 2				x	x	
4	0 + 4			x			x
5	1 + 4			x		x	
6	2 + 4			x	x		
7	0 + 7		x				x
8	1 + 7		x			x	
9	2 + 7		x		x		
10	3 + 7		x	x			
11	0 + 11	x					x
12	1 + 11	x				x	
13	2 + 11	x			x		
14	3 + 11	x		x			
15	4 + 11	x	x				

CANCELLED

CONTROL CHANNEL ADDRESS CODES OVERLEAF

bitpositions 7 6 5 4 3 2 1 0

hexadecimals

second hexadecimals ↓ first hexadecimals →

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	IOU	TAC		ASU			SSU 0	SSU 1								
1	CST 02				TRP	TRP	TU	FD								STB
2	CST 04	ML			TRL											
3																
4									CST 09	MT						
5																
6																
7																
8																
9	CST 18	SD			TU AJ.BU	TU IT.OT	TU SE.L	TU SE.R					FD AJ.BU	FD IT.OT	FD SE.L	FD SE.R
A																
B																
C																
D																
E																
F																

FIXED ADDRESSES:

IOU = Input-Output Unit

TAC = Test Access Circuit

ASU = Alarm and Switching Unit

SSU = Subsystem Switching Unit

STB = Scan Transfer Buffer

TRP = Paper Tape Reader Punch

TRU =

CONTROL CHANNEL ADDRESS CODES TEST FLOOR

8 5 4 1 bitpositions

2	1	hexadecimals

second hexadecimals ↓ first hexadecimals →

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	IOU	TAC		ASU			SSU 0	SSU 1								
1	CST 02				TEP	TRP	TU	FD								STB
2	CST 04	ML			TRL											
3																
4																
5																
6	CST 12	TIM			TEP	TRP							CC			
7	CST 14	SP			TU AJ.BJ	TU IT.ØT	TU ABIØ	TU ABIØ					FD AJ.BJ	FD IT.ØT	FD ABIØ	FD ABIØ
8	CST 16 *	MT			TU SR.L	TU SR.R							FD SR.L	FD SR.R		
9	CST 18 *	MT			TU SR.L	TU SR.R							FD SR.L	FD SR.R		
A																
B																
C																
D																
E																
F																

FIXED ADDRESSES:

IOU = Input-Output Unit

TAC = Test Access Circuit

ASU = Alarm and Switching Unit

SSU = Subsystem Switching Unit

STB = Scan Transfer Buffer

TRP = Paper Tape Reader/Punch

* CST/MT and associated Subsystems are addressed CST16 or 18 by means of a switch

16+2=32
32-3=29 octaal

DATA CHANNEL ADDRESS CODES

Overvecht

Control Words in Memory

Location:

810	CW00	ISC command
811	CW01	Status DM
81C	CW02	Command Formatting
81D	CW03	Command Formatting
81E	CW04	Command Formatting
81F	CW05	Command Formatting
816	CW01	Status DCC

Subsystem Addresses

SS address:	Subsystem	
1	MTS 1	Magnetic Tape Subsystem 1
2	MTS 2	Magnetic Tape Subsystem 2
6	LPS	Line Printer Subsystem.

Data Channel Addresses in the ISC

0XXX	DC0
1001	DM1 (High Speed Utility)

Cleaned and updated

DATA CHANNEL ADDRESS CODES

LAB. TESTFLOOR

Control Words in Memory

LOCATION:		CONTENTS:	DCH addr.:
082C	CW1C	BCH-0	0
082D	CW1D	BCH-0	
082E	CW1E	BCH-0	
082F	CW1F	BCH-0	
081C	CW1C	DCH	6
0811	CWO1	DCC-Status	(bit 4 of ISC=0)
0812	CW [illegible]	BCH-0	
0813	CWO1	BCH-0	
0814	CWOC	DCH	
0815	CWO1	DCH	
0818	CWOC	BCH-1	1
0819	CWO1	BCH-1	
081C	CW1C	BCH-1	
081D	CW1D	BCH-1	
081E	CW1E	BCH-1	
081F	CW1F	BCH-1	

Subsystem Addresses

SS address:	Subsystem	
0	-	
1	MTS1	Magnetic Tape Subsystem 1
2	MTS2	Magnetic Tape Subsystem 2
3	MTS3	Magnetic Tape Subsystem 3
4	-	
5	DSCS	Disk Subsystem
6	LPS	Line Printer Subsystem
7	-	

Cancelled

DATA CHANNEL ADDRESS CODES

LAB. TESTFLOOR

Control Words in Memory

LOCATION:	CONTENTS:		DCH addr.:
082C	CW1C	BCH-0	0
082D	CW1D	BCH-0	
082E	CW1E	BCH-0	
082F	CW1F	BCH-0	
081C	CW1C	DCH	6
0811	CW01	DCC-Status	(bit 4 of ISC=0)
0812	CW00	BCH-0	
0813	CW01	BCH-0	
0814	CW00	DCH	
0815	CW01	DCH	
0812	CW00	BCH-1	1
0813	CW01	BCH-1	
082C	CW1C	BCH-1	
082D	CW1D	BCH-1	
082E	CW1E	BCH-1	
082F	CW1F	BCH-1	

Subsystem Addresses

DCH address:	Subsystem	
0	-	
1	MTS1	Magnetic Tape Subsystem 1
2	MTS2	Magnetic Tape Subsystem 2
3	MTS3	Magnetic Tape Subsystem 3
4	-	
5	DSCS	Disk Subsystem
6	LPS	Line Printer Subsystem
7	-	

Cancelled

INTERRUPT ALLOCATION

INP.	GROUP 1	GROUP 2	GROUP 3	GROUP 4
1	PRE-0	DS-0	IO-0	-
2	PRE-1	DS-1	IO-1	-
3	OK-0 - -	-	CPT	RTC-0
4	OK-1 - -	-	DE-0 DS-0	RTC-1
5	- - OK-0	-	DE-1 DS-1	-
6	- - OK-1	-	CST-0.0 CST-1.0	-
7	- -	-	CST-0.1 CST-1.1	-
8	TEST-1	TEST-2	TEST-3	TEST-4
9	-		CST-0.2 CST-1.2	
10	-		DS-0 DE-0	
11	-		2 DS-1 DE-1	
12	-		-	
13	-		-	
14	-		-	
15	-		-	
16	-		-	

INP	GROUP 5	GROUP 6	GROUP 7	GROUP 8
1	EOS-0	SBE-0	KB-RY (CCH)	SCINT0
2	EOS-1	-	KB-ER ,,	SCINT1
3	-	SBE-1	PI-RY ,,	SBE-0
4	-	-	PTP-RY ,,	SBE-1
5	-	-	PTR-RY ,,	-
6	-	-	PTR-ER ,,	-
7	-	-	TOD-INT	-
8	TEST-5	TEST -6	TEST-7	TEST-8
9	-		-	
10	-		-	
11	-		-	
12	-		-	
13	-		-	
14	-		-	
15	-		-	
16	-		-	

Note: If inputs of IA0 and IA1 are different, the left indication refers to IA0, the right indication to IA1.

INTERRUPT ALLOCATION

INP.	GROUP 1	GROUP 2	GROUP 3	GROUP 4
1	PRE-0	-	IO-0	-
2	PRE-1	-	IO-1	-
3	OK-0 - -	-	CPT	RTC-0
4	OK-1 - -	-	DE-0	RTC-1
5	- - OK-0	-	DE-1	-
6	- - OK-1	-	CST-0.0 CST-1.0	-
7	-	-	CST-0.1 CST-1.1	-
8	TEST-1	TEST-2	TEST-3	TEST-4
9	-		CST-0.2 CST-1.2	
10	-		-	
11	-		-	
12	-		-	
13	-		-	
14	-		-	
15	-		-	
16	-		-	

INP	GROUP 5	GROUP 6	GROUP 7	GROUP 8
1	EOS-0	-	KB-RY (CCH)	SCINT0
2	EOS-1	-	KB-ER ,,	SCINT1
3	-	-	PI-RY ,,	-
4	-	-	PTP-RY ,,	-
5	-	-	PTR-RY ,,	-
6	-	-	PTR-ER ,,	-
7	-	-	TOD-INT	-
8	TEST-5	TEST -6	TEST-7	TEST-8
9	-		-	
10	-		-	
11	-		-	
12	-		-	
13	-		-	
14	-		-	
15	-		-	
16	-		-	

Note: If inputs of IA0 and IA1 are different, the left indication refers to IA0, the right indication to IA1.

INTERRUPT ALLOCATION - TESTFLOOR

LEFT INDICATION: PT-0, RIGHT INDICATION: PT-1

INP	GROUP 1	GROUP 2	GROUP 3	GROUP 4
1	PRE-0	-	IO-0	-
2	PRE-1	-	IO-1	-
3	OK-0 -	-	CPT	RTC-0
4	OK-1 -	-	DE-0	RTC-1
5	- OK-0	-	DE-1	-
6	- OK-1	-	CCH0.0 CCH1.0	-
7	-	-	-	-
8	TEST-1	TEST-2	TEST-3	TEST-4
9	-	-	-	-
10	-	-	-	-
11	-	-	-	-
12	-	-	-	-
13	-	-	-	-
14	-	-	-	-
15	-	-	-	-
16	-	-	-	-

INP	GROUP 5	GROUP 6	GROUP 7	GROUP 8
1	EOS-0	-	KB-RY 3)	SCINT-0
2	EOS-1	DM0 (BCH-0)	KB-ER 3)	SCINT-1
3	-	-	PI-RY 3)	RTC 1) -
4	-	DM1 (BCH-1)	PTP-RY 3)	OK 1) -
5	-	-	PTR-RY 3)	P.ER.Da. 1) -
6	-	-	PTR-ER 3)	P.ER.Add. 1) -
7	-	-	TOD	E.SEL. 1) -
8	TEST-5	TEST-6	TEST-7	TEST-8
9	-	-	KB-RY 2) -	ACT. 1) -
10	-	-	KB-ER 2) -	TIM. 1) -
11	-	-	PI-RY 2) -	24 HOUR INT.
12	-	-	PTP-RY 2) -	-
13	-	-	PTR-RY 2) -	-
14	-	-	PTR-ER 2) -	-
15	-	-	-	-
16	-	-	-	-

Request staticiser cards present at positions C23, C25, C29 (for LSU-0 on DCH and System Test Coupler interrupts).
For PT-0 also at position C27 for LSU-0 accessed via CCH-0.

1) Interrupts of System Test Coupler.

2) Interrupts of LSU-0, accessed via CCH-0, (CSTG12)

3) Interrupts of LSU-0, accessed via CCH-0 if "SEPARATED" system (CSTG02)
" " LSU-1, " " CCH-1 " " " (CSTG02)
" " LSU-1, " " CCH-0 and -1 if "NORMAL" system (CSTG02)

SSU ALLOCATIONS

Bit position of Out-data field of OTF to SSU

	16	15	14	13	12	11	10	9	1 ÷ 4 HEXA-DEC.	SSU REL. DR. CARD POSITION
BRANCH 0 OF CCH	IN 114	OUT 113	IN 212	OUT 211	IN 112	OUT 111	IN 210	OUT 209	0	61
* COMMON EQ. RACK				SP. 211	SP. 112	TOD 111	C-TRP 210	C-TEP 209	1	
UNASSIGNED (NOT WIRED)	SP.	SP.	SP.							
LEVEL OF TEST INT.	8	7	6	5	4	3	2	1	2	
Note: set-test interr. should be preceeded by a reset!										
BRANCH 0 OF CCH	IN 118	OUT 117	IN 216	OUT 215	IN 116	OUT 115	IN 214	OUT 213	3	63
					IN 120	OUT 119	IN 218	OUT 217	4	
BRANCH 1 OF CCH	IN 112	OUT 111	IN 210	OUT 209						
NR. OF DCH (INTERR.)	7	6	5	4	3	2	1	0	5	
BRANCH 1 OF CCH	IN 116	OUT 115	IN 214	OUT 213	IN 114	OUT 113	IN 212	OUT 211	6	65
	IN 120	OUT 119	IN 218	OUT 217	IN 118	OUT 117	IN 216	OUT 215	7	
UNASSIGNED (NOT WIRED)	SP.	SP.	SP.	SP.	SP.	SP.	SP.	SP.	8	
BRANCH 2 OF CCH	IN 114	OUT 113	IN 212	OUT 211	IN 112	OUT 111	IN 210	OUT 209	9	67
	IN 118	OUT 117	IN 216	OUT 215	IN 116	OUT 115	IN 214	OUT 213	A	
					IN 120	OUT 119	IN 218	OUT 217	B	
UNASSIGNED (NOT WIRED)	SP.	SP.	SP.	SP.						

The numbers below (SSU) IN, (SSU) OUT or SP (ARE) refer to the pin positio in the outbus connector or miscellaneous rack connector in the PT.

CANCELLED

SSU ALLOCATIONS OVERVECHT

bit pos. 9 - 16	bits 1 - 4 hexa dec. group code	SSU function	CST group	CONNECTOR AT PT/CST	Strapped to CST-Outbus connector
				Outbus CCH	
9	0	out CST	CSTG02	pin 209	pin 221
10	0	in CST	CSTG02	pin 210	pin 222
				Misc. Rack	
9	1	out CTEP	CSTG02	pin 209	-
10	1	out CTRP	CSTG02	pin 210	-
11	1	out TOD	CSTG02	pin 111	-
				Outbus CCH	
11	0	out CST	CSTG04	pin 111	pin 221
12	0	in CST	CSTG04	pin 112	pin 222
13	0	out CST	CSTG09	pin 211	pin 221
14	0	in CST	CSTG09	pin 212	pin 222
15	0	out CST	CSTG18	pin 113	pin 221
16	0	in CST	CSTG18	pin 114	pin 222
10	5	in DM-1 INT.	-	INTERNAL	-

Relay driver cards present at positions 61, 63.

SSU ALLOCATIONS TESTFLOOR

bit pos. 9 - 16	bits 1 - 4 hexa dec. group code	SSU function	CST group	CONNECTOR AT PT/CST	Strapped to CST-Outbus connector
				Outbus CCH	
9	0	out CST	CSTG02	pin 209	pin 221
10	0	in CST	CSTG02	pin 210	pin 222
13	0	out CST	CSTG04	pin 211	pin 221
14	0	in CST	CSTG04	pin 212	pin 222
13	3	out CST	CSTG12	pin 215	pin 221
14	3	in CST	CSTG12	pin 216	pin 222
11	0	out CST	CSTG14	pin 111	pin 221
12	0	in CST	CSTG14	pin 112	pin 222
9/11 3)	3	out CST	CSTG16/18	pin 213/115	pin 221
10/12	3	in CST	CSTG16/18	pin 214/116	pin 222
9—16	2	Test int.		INTERNAL	
9	5	DM-0 int.		INTERNAL	-
10	5	DM-1 int.		INTERNAL	-
15	5	DM-6 int.		INTERNAL 1)	-
9	1	out CTEP	CSTG02	pin 209 2)	-
10	1	out CTRP	CSTG02	pin 210 2)	-
9	4	out CTEP	CSTG12	pin 217	pin 123
10	4	out CTRP	CSTG12	pin 218	pin 124
11	1	out TOD		pin 111 2)	-

1) And external interrupts of DCH-LSU-0

2) Pins of CE Utility Interrupt connector

3) SSU position for CSTG16 or 18 is realised by a switch
Relay driver cards present at position 61, 63